FIG. 1

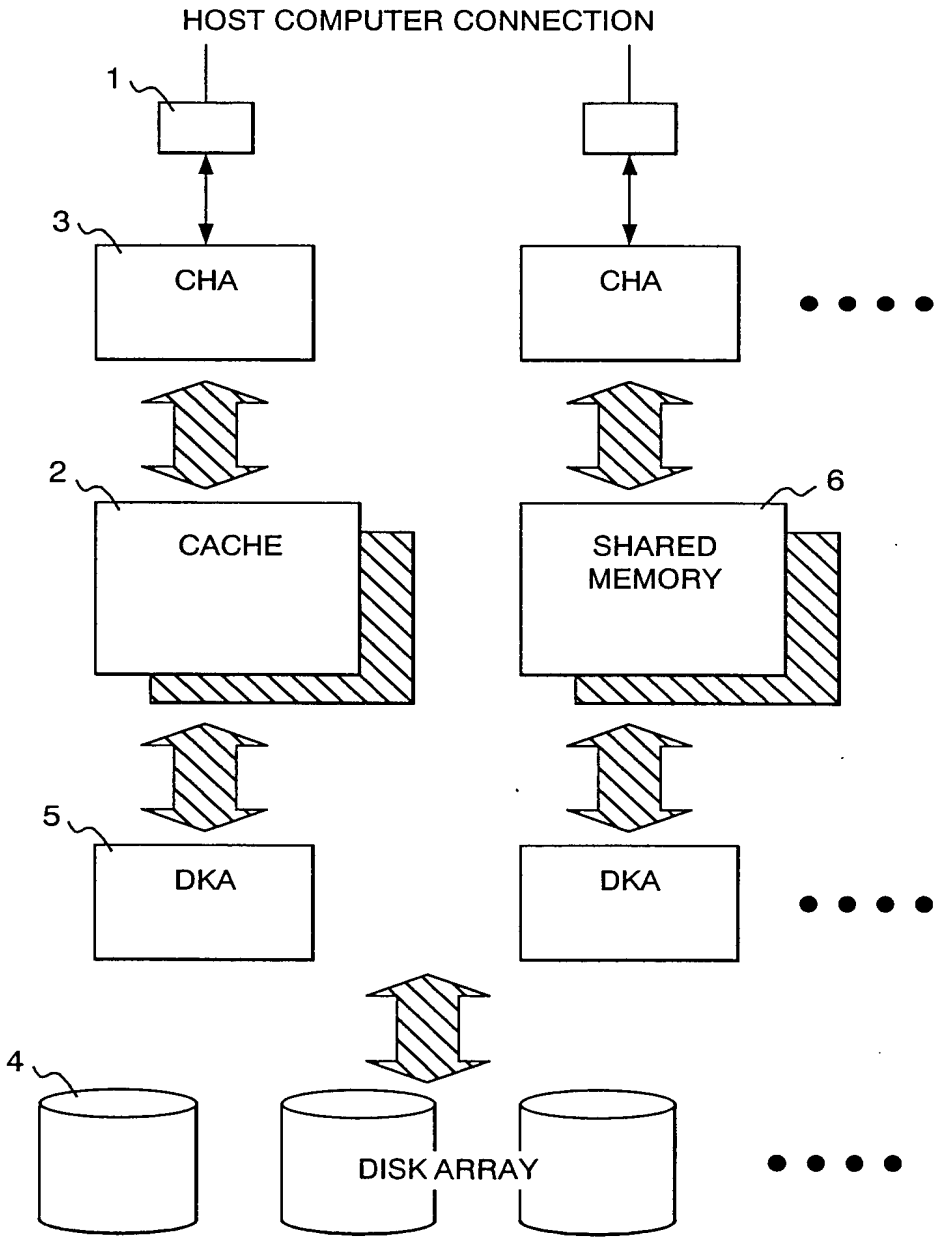

HOST COMPUTER CONNECTION
1
3
CHA
CHA
2
CACHE
6
SHARED MEMORY
5
DKA
DKA
4
DISK ARRAY

FIG. 2

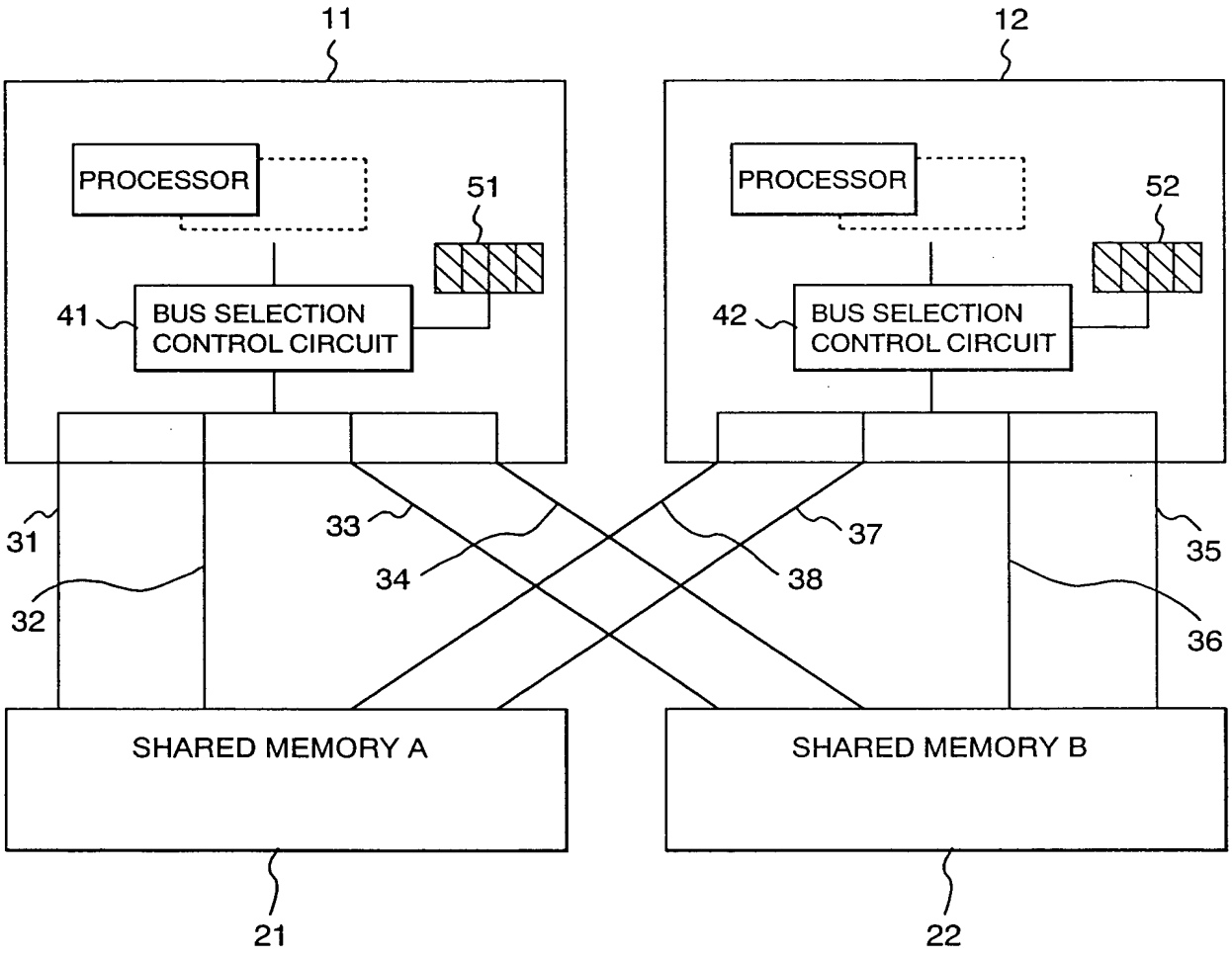

11
12
PROCESSOR
PROCESSOR
51
52
41
BUS SELECTION CONTROL CIRCUIT
42
BUS SELECTION CONTROL CIRCUIT
31
32
33
34
37
38
35
36
SHARED MEMORY A
SHARED MEMORY B
21
22

FIG. 3

SET VALUE OF EACH BIT OF THE REGISTER				ACCESS PATH
A-1	A-2	B-1	B-2	
0	0	0	0	PLANE A = DISTRIBUTED PATH, PLANE B = DISTRIBUTED PATH
1	0	0	0	PLANE A = USES PATH A-1, PLANE B = DISTRIBUTED PATH
0	1	0	0	PLANE A = USES PATH A-2, PLANE B = DISTRIBUTED PATH
0	0	1	0	PLANE A = DISTRIBUTED PATH, PLANE B = USES PATH B-1
0	0	0	1	PLANE A = DISTRIBUTED PATH, PLANE B = USES PATH B-2
1	0	1	0	PLANE A = USES PATH A-1, PLANE B = USES PATH B-1
1	0	0	1	PLANE A = USES PATH A-1, PLANE B = USES PATH B-2
0	1	1	0	PLANE A = USES PATH A-2, PLANE B = USES PATH B-1
0	1	0	1	PLANE A = USES PATH A-2, PLANE B = USES PATH B-2

FIG. 4

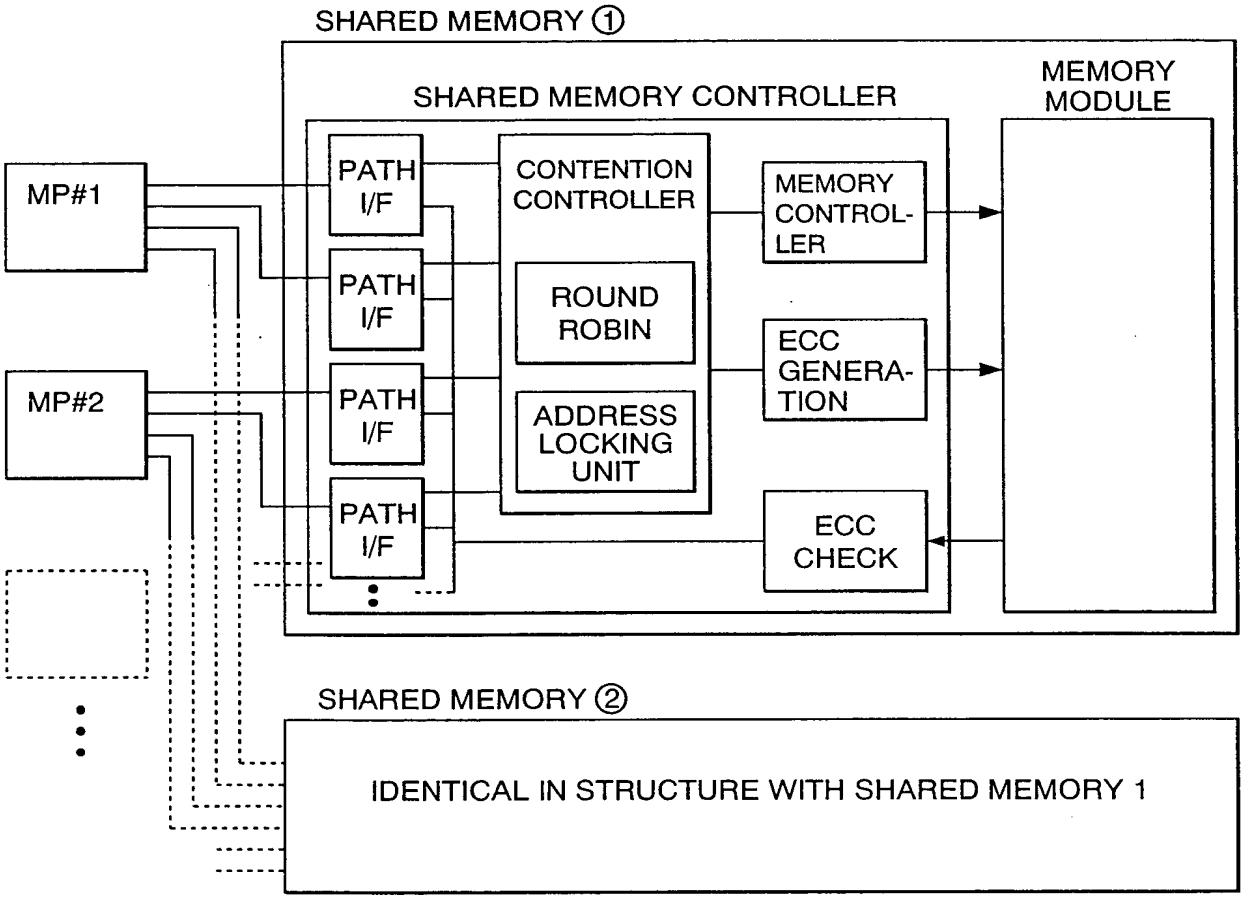

SHARED MEMORY ①
SHARED MEMORY CONTROLLER
MEMORY MODULE
MP#1
MP#2
PATH I/F
PATH I/F
PATH I/F
PATH I/F
CONTENTION CONTROLLER
ROUND ROBIN
ADDRESS LOCKING UNIT
MEMORY CONTROL-LER
ECC GENERA-TION
ECC CHECK
SHARED MEMORY ②
IDENTICAL IN STRUCTURE WITH SHARED MEMORY 1

FIG. 5

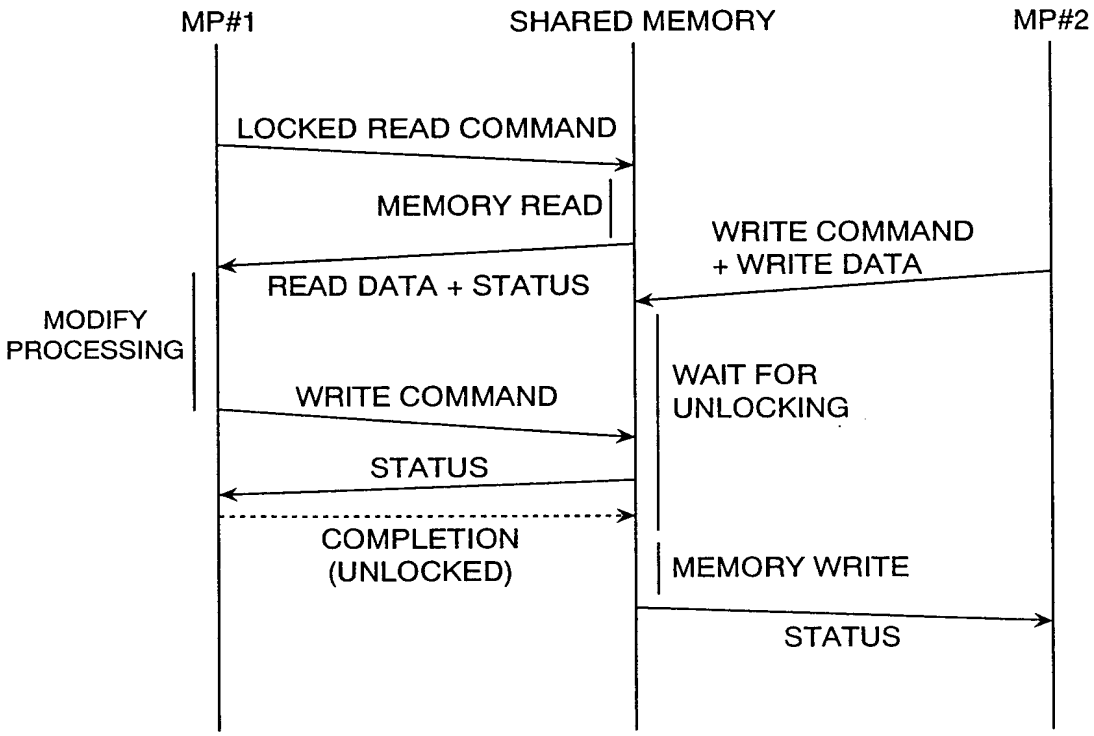
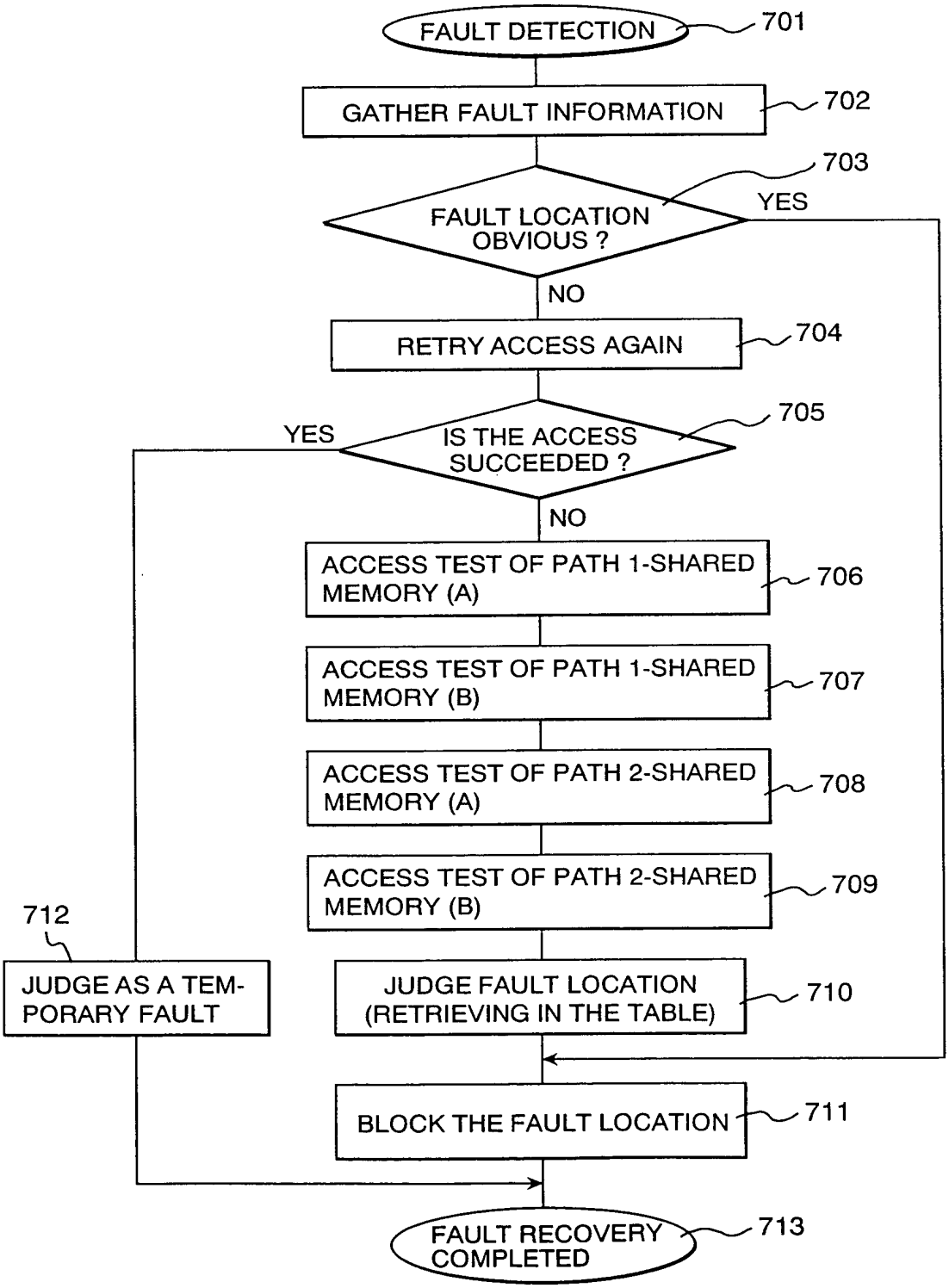

MP#1
SHARED MEMORY
MP#2
LOCKED READ COMMAND
MEMORY READ
WRITE COMMAND
+ WRITE DATA
READ DATA + STATUS
MODIFY
PROCESSING
WAIT FOR
UNLOCKING
WRITE COMMAND
STATUS
COMPLETION
(UNLOCKED)
MEMORY WRITE
STATUS

FIG. 6

ACCESS TEST RESULTS				ASSUMED FAULT LOCATION
PATH 1A (a)	PATH 1A (b)	PATH 1B (a)	PATH 1B (b)	
OK	OK	OK	OK	NO FAULT
NG	OK	OK	OK	PATH 1A (a)
OK	NG	OK	OK	PATH 1A (b)
OK	OK	NG	OK	PATH 1B (a)
OK	OK	OK	NG	PATH 1B (b)
NG	NG	OK	OK	SHARED MEMORY A
NG	OK	NG	OK	FAULT MULTIPLEXED ? (PROCESSOR)
NG	OK	OK	NG	FAULT MULTIPLEXED ? (PROCESSOR)
OK	NG	NG	OK	FAULT MULTIPLEXED ? (PROCESSOR)
OK	NG	OK	NG	FAULT MULTIPLEXED ? (PROCESSOR)
OK	OK	NG	NG	SHARED MEMORY B
NG	NG	NG	OK	FAULT MULTIPLEXED ? (PROCESSOR)
NG	NG	OK	NG	FAULT MULTIPLEXED ? (PROCESSOR)
NG	OK	NG	NG	FAULT MULTIPLEXED ? (PROCESSOR)
OK	NG	NG	NG	FAULT MULTIPLEXED ? (PROCESSOR)
NG	NG	NG	NG	PROCESSOR

FIG. 7


FAULT DETECTION
701
GATHER FAULT INFORMATION
702
703
FAULT LOCATION OBVIOUS ?
YES
NO
RETRY ACCESS AGAIN
704
705
YES
IS THE ACCESS SUCCEEDED ?
NO
ACCESS TEST OF PATH 1-SHARED MEMORY (A)
706
ACCESS TEST OF PATH 1-SHARED MEMORY (B)
707
ACCESS TEST OF PATH 2-SHARED MEMORY (A)
708
ACCESS TEST OF PATH 2-SHARED MEMORY (B)
709
712
JUDGE AS A TEMPORARY FAULT
JUDGE FAULT LOCATION (RETRIEVING IN THE TABLE)
710
BLOCK THE FAULT LOCATION
711
FAULT RECOVERY COMPLETED
713